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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/511,566	04/13/2005	Jurgen Leib	2133.063USU	4191

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EXAMINER	
ARENA, ANDREW OWENS	

ART UNIT	PAPER NUMBER
2811	

MAIL DATE	DELIVERY MODE
06/14/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/511,566	LEIB ET AL.	
	Examiner	Art Unit	
	Andrew O. Arena	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 March 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32 and 34-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32 and 34-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 03/20/2007 has been entered.

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 102

Claims 23, 26, 27, and 29-32 are rejected under 35 U.S.C. 102(b) as being anticipated by Wada (US 2002/0019069).

Re claim 23, Wada discloses (Fig 1) an electronic module (1) comprising:

a substrate (6) having a first substrate side (B) and a second substrate side (A) opposite to the first substrate side (¶73 ln 6);

one or more connection structures (2+8 in region of 2; see Fig 8A; ¶98 ln 4-6) being disposed on the first substrate side (¶73 ln 4-5);

a glass layer (11+9; ¶75 ln 5-8) being on the first substrate side; and

a plurality of etched pits (4) and line contacts (8) being defined in the second substrate side (¶74), the plurality of etched pits extending through the substrate and stopping at the one or more connections structures.

The product-by-process limitation "vapor deposited" does not structurally distinguish the claimed product from the applied art. See MPEP § 2113.

Re claim 26, Wada discloses the second substrate side is thinned (interpreted - the desired thinness).

The product-by-process limitation "after the glass layer is deposited on the first substrate side" does not structurally distinguish the claimed product from the applied art. See MPEP § 2113.

Re claim 27, Wada discloses (Fig 9) a passivation layer (26; ¶136 In 5) on the second substrate side.

Re claim 29, Wada discloses the glass layer comprises a plurality of glass layers (11, 9; ¶75 In 5-8).

Re claim 30, Wada discloses the individual layers (11, 9) of the plurality of glass layers have different compositions (low melting point glass versus optical glass).

Re claim 31, Wada discloses (Fig 1) line contacts (8) that are connected to the one or more semiconductor structures (¶74 In 6-8) on the first substrate side.

Re claim 32, Wada discloses (Fig 1) a ball grid array (24) at the line contacts.

Claim Rejections - 35 USC § 103

Claim 24 is rejected under 35 U.S.C. 103(a) as being obvious in view of Wada as applied to claim 23 above, and further in view of Camlibel (US 4,374,391).

Re claim 24, Wada differs from the claimed invention only in not disclosing a second glass layer on the second substrate side.

Camlibel discloses (Fig 5) an analogous device (60) having the first and the opposite second sides both covered with glass layers (62, 68; col 5 ln 63 – col 6 ln 2), which protects the surface (col 3 ln 46).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Wada in view of Camlibel by depositing a glass layer on the second substrate side; at least to protect the surface.

Claim 25 is rejected under 35 U.S.C. 103(a) as being obvious in view of Wada.

Re claim 25, Wada discloses (Fig 1) an electronic module (1) comprising: a substrate (6) having a first substrate side (B) and a second substrate side (A) opposite to the first substrate side (¶73 ln 6);

one or more connection structures (2+8 in region of 2; see Fig 8A; ¶98 ln 4-6) being disposed on the first substrate side (¶73 ln 4-5);

a glass layer (9; ¶75 ln 5-6) being on the first substrate side;

a plastic layer (11; ¶75 ln 7) on a surface of the glass layer; and

a plurality of etched pits (4) and line contacts (8) being defined in the second substrate side (¶74), the plurality of etched pits extending through the substrate and stopping at the one or more connections structures.

The product-by-process limitation "deposited" does not structurally distinguish the claimed product from the applied art. See MPEP § 2113.

Wada differs from the claimed invention only in not disclosing said plastic layer on a surface of the glass layer opposite the substrate.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to reverse/rearrange the order of the glass layer and plastic layer; which would not modify the device operation. See MPEP § 2144.04(VI)(A&C).

If objective evidence is made of record that establishes either: that the facts in the above referenced legal decisions are not sufficiently similar to the present application; or that there is criticality to the order of parts as claimed, then the following alternate grounds of rejection of claim 25 applies.

Claim 25 is rejected under 35 U.S.C. 103(a) as being obvious in view of Wada, Camlibel, and Xu (US 6,111,270).

Re claim 25, Wada differs from the claimed invention only in not disclosing said plastic layer on a surface of the glass layer opposite the substrate.

Xu discloses (e.g., Fig 2) a dielectric stack of layers (16) having different indexes of refraction forming a dielectric mirror (col 3 ln 35-44), i.e., designed reflection control.

Camlibel discloses using glass layers both as a dielectric mirror and to reduce reflection (col 3 ln 40-56, esp. ln 51-54) , i.e., designed reflection control.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Wada in view of Camlibel and Xu to comprise a plastic layer on a surface of the glass layer opposite the substrate; at least to reduce surface reflection. See also MPEP § 2141.03 (reflection control as applicable principle).

Claim 28 is rejected under 35 U.S.C. 103(a) as being obvious in view of Wada as applied to claim 23 above in further view of Butt (US 4,889,960).

Re claim 28, Wada differs from the claimed invention in not disclosing the glass layer comprises a mixed layer of inorganic and organic constituents.

Butt discloses (Fig 1) electronic modules encapsulated with organic-reinforced glass (col 2 ln 67 - col 3 ln 6) to reinforce the glass (col 5 ln 11-15).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Wada in view of Butt wherein the glass layer comprises a mixed layer of inorganic and organic constituents; at least for reinforcement.

Claims 1-7, 9-21, 34, and 35-40 are rejected under 35 U.S.C. 103(a) as being obvious in view of Wada, Camlibel, and Fleming (US 5,047,369).

Re claim 1, Wada discloses (Figs 6-9) a process for forming a housing for electronic modules, comprising the steps of:

providing a substrate (5; ¶83 ln 1-2) having one or more regions, the one or more regions having a structure (surface exposed at 50, e.g., Fig 6F) selected from the group consisting of structures for forming semiconductor structures and structures for forming connection structures (may be regarded as either), the substrate having at least a first substrate side (B; ¶84 ln 1-3) to be encapsulated and an underside (A);

providing a glass source (¶113);

arranging the first substrate side in such a manner with respect to the glass source that the first substrate side can be coated (¶113);

coating the first substrate side with a glass layer (Fig 9: 9; ¶113 ln 1-2);

thinning the substrate (interpreted - making to the desired thinness; inherent) on the underside;

using the structure as an etching stop (Fig 6E-6F: etching stops at said structure; ¶89-¶90) while producing etching pits (Fig 6E-7G: 4; ¶93 ln 1-2) on the underside, so that the etching pits extend through the substrate to the structure (e.g., Figs 7B-9); and

producing line contacts (Fig 8A: 8a; Fig 9: 18) on the underside.

Wada differs from the claimed invention only in not disclosing vapor-deposition.

Camlibel teaches that glass encapsulation is particularly desirable in integrated circuits such as that of Wada (col 1 ln 33-35, col 2 ln 50, col 3 ln 8-10) and that e-beam (vapor) deposition is known in the art to be a suitable technique (col 4 ln 44-47).

Fleming teaches that glass encapsulation is particularly desirable in integrated circuits such as that of Wada (col 1 ln 63-67, col 3 ln 12-14) and that e-beam (vapor) deposition is a preferred technique, at least for reduced contamination (col 1 ln 28-32).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Wada in view of Camlibel and Fleming such that said glass source is a vapor-deposition glass source and that said coating is vapor-coating; at least for reduced contamination.

Furthermore, it is generally considered obvious to choose what is already known in the art to be suitable for a given purpose. See MPEP § 2144.06 and 2144.07.

Re claim 2, Wada discloses (Fig 9) the one or more regions are arranged on the first substrate side (¶84 In 1-3).

Re claim 3, Wada discloses (Fig 9) providing the substrate with a passivation layer (26; ¶136 In 5) on a second side (A) that is on the opposite side from the first substrate side (B).

Re claim 4, Wada discloses the substrate comprises a wafer (5; ¶83 In 2), the process further comprising packaging components which still form part of the wafer (¶124 In 1-5).

Re claim 5, Wada discloses coating a second substrate side with a protective film (26; ¶136 In 5).

Wada differs from the claimed invention in not disclosing vapor-coating a second substrate side with a glass layer.

Camlibel discloses (Fig 5) an analogous device (60) having the first and the opposite second sides both covered with glass layers (62, 68; col 5 In 63 – col 6 In 2), which protects the surface (col 3 In 46).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to further modify Wada in view of Camlibel to further comprising vapor-coating a second substrate side with a glass layer; at least for protection.

Re claim 6, Wada as modified above discloses the vapor-deposition glass source generates at least a binary glass system (borosilicate: Camlibel col 2 In 55).

Re claim 7, Wada as modified above discloses the first substrate side is vapor-coated until the glass layer has a thickness in the range from 0.01 to 1000 pm (Camlibel col 7 In 68; 3000 Angstroms = 0.3 pm).

Re claim 9, Wada as modified above discloses the glass layer has a thickness in the range between 0.1 and 50 IJm (Camlibel col 7 In 68).

Re claim 10, Wada as modified above differs from the claimed invention only in not expressly disclosing a glass layer thickness in the range between 50 and 200 IJm. Parameters such as film thickness in the art of semiconductor manufacturing are subject to routine experimentation and optimization. It would have been obvious to one of ordinary skill in the art at the time the invention was made that the glass layer have a thickness in the range between 50 and 200 IJm; at least to optimize the glass layer's optical properties.

Re claim 11, Wada as modified above discloses generating a vapor from a glass target by means of an electron beam (inherent in e-beam; Camlibel col 4 In 47).

Re claim 12, Wada as modified above does not limit the borosilicate glass to any particular type, therefore the combined disclosure encompasses all well-known

borosilicate glass types, including those containing aluminum oxide and alkali metal oxide fractions.

Re claim 13, Wada as modified above discloses the glass layer has a coefficient of thermal expansion that is virtually equal to that of the substrate (Camlibel: col 2 In 57-62; Fig 1, col 5 In 7-18).

Re claim 14, Wada as modified above discloses the glass layer provides a hermetic (air-tight) seal.

Re claim 15, Wada discloses coating a second substrate side with a protective film (26; ¶136 In 5).

Wada differs from the claimed invention in not disclosing vapor-coating a second substrate side with a glass layer.

Camlibel discloses (Fig 5) an analogous device (60) having the first and the opposite second sides both covered with glass layers (62, 68; col 5 In 63 – col 6 In 2), which protects the surface (col 3 In 46).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to further modify Wada in view of Camlibel to further comprising vapor-coating a second substrate side with a glass layer; at least for protection.

This combination comprises vapor depositing a plurality of glass layers onto (at least one onto the top of and at least one onto the bottom of) the substrate.

Re claim 16, Wada discloses (Fig 6F-6G) removing material from a second substrate side (¶91 In 1-2), the second substrate side being on the opposite side from the first substrate side.

Re claim 17, Wada discloses (Fig 3) the substrate includes a wafer (5) having a plurality of the structures (3; ¶83 ln 1-2) wherein the process further comprises dividing the wafer to form a plurality of electronic modules which each have first encapsulated sides (¶124 ln 1-5).

Re claim 18, Wada discloses (Fig 9) providing the underside with a plastic covering (26; ¶135) while leaving clear the ball grid array (24).

Re claim 19, Wada as modified above discloses vapor coating the underside with the glass layer (Fig 11: 26) after the plastic layers (Fig 7F: 66) have been removed from the underside so that the plurality of electronic modules are encapsulated on both sides.

Re claim 20, Wada as modified above differs from the claimed invention only in not expressly disclosing the glass layer on the underside has a thickness in the range from 1 to 50 μm.

Parameters such as film thickness in the art of semiconductor manufacturing are subject to routine experimentation and optimization.

It would have been obvious to one of ordinary skill in the art at the time the invention was made that the glass layer have a thickness in the range from 1 to 50; at least to optimize the glass layer's optical properties.

Re claim 21, Wada discloses (Fig 8A) filling in (interpreted as providing some amount of some filler) the etching pits with conductive material (8; ¶98 ln 4-5).

Re claim 34, Wada discloses (e.g., Fig 9) applying a layer of plastic (11) below the glass layer (9; ¶75 ln 5-7).

Wada differs from the claimed invention only in not disclosing said plastic layer on a surface of the glass layer opposite the substrate.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to reverse/rearrange the order of the glass layer and plastic layer; which would not modify the device operation. See MPEP § 2144.04(VI)(A&C).

Re claim 35, Wada discloses the plurality of glass layers have the same or various glass compositions.

Re claim 36, Wada discloses the etching pits are produced on the underside opposite the structure (Fig 8A: pits 4 are on underside A).

Re claim 37, Wada discloses the line contacts are produced on the underside opposite the structure (Fig 8A: contacts 8a are on underside A).

Re claim 38, Wada discloses (Fig 9) applying a ball grid array at the line contacts (24; col ¶137 ln 2).

Re claim 39, Wada discloses (Figs 6) lithographing ([0085], [0089]) plastic layers (32, 42, 44) on the substrate to define the structure and removing the plastic layers from the underside (Fig 6F-6G: 44; ¶91 ln 1-2).

Re claim 40, Wada as modified above discloses (Fig 11A-11B) uncovering the line contacts (18, 22) by local elimination of the glass layers (from Fig 11A to 11B).

Claim 8 is rejected under 35 U.S.C. 103(a) as being obvious is view of Wada, Camlibel, and Fleming as applied to claim 1 above, and further in view of Butt.

Re claim 8, Wada as modified above does not disclose organic constituents.

Butt discloses that an organic-reinforced glass is particularly reliable and useful for hermetic sealing of electronic packages (col 2 ln 67 – col 3 ln 6, col 5 ln 11-17).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to further modify Wada in view of Butt by providing a reservoir having organic constituents and converting the organic constituents into the vapor state through the application of a vacuum so that during the vapor-coating mixed layers comprising inorganic and organic constituents can be formed on the first substrate side; at least for reliability.

Claim 22 is rejected under 35 U.S.C. 103(a) as being obvious in view of Wada, Camlibel, and Fleming as applied to claim 1 above, and further in view of Miles (US 2005/0244949).

Re claim 22, Wada as modified above differs from the claimed invention in not disclosing plasma ion assisted deposition.

Miles discloses ion assisted e-beam deposition controls stress (¶189 ln 11).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to further modify Wada in view of Miles by using ion assisted e-beam deposition in place of conventional e-beam deposition; at least to control stress.

If objective evidence is made of record that establishes either: that the facts in the above referenced legal decisions are not sufficiently similar to the present

application; or that there is criticality to the order of parts as claimed, then the following alternate grounds of rejection of claim 34 applies.

Claim 34 is rejected under 35 U.S.C. 103(a) as being obvious in view of Wada, Camlibel, and Fleming, as applied to claim 1 above, and further in view of Xu.

Re claim 34, Wada differs from the claimed invention only in not disclosing said plastic layer above the glass layer.

Xu discloses (e.g., Fig 2) a dielectric stack of layers (16) having different indexes of refraction forming a dielectric mirror (col 3 ln 35-44), i.e., designed reflection control.

Camlibel discloses using glass layers both as a dielectric mirror and to reduce reflection (col 3 ln 40-56, esp. ln 51-54) , i.e., designed reflection control.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Wada in view of Camlibel and Xu to comprise applying a layer of plastic above the glass layer; at least to reduce surface reflection. See also MPEP § 2141.03 (reflection control as applicable principle).

Response to Arguments

Applicant's arguments filed 03/20/2007 have been fully considered but they are not persuasive and/or are moot in view of the new interpretations and new citations.

The arguments regarding claims 1, 23, and 35 are not convincing. The claim language "a structure selected from the group..." encompasses Wada's disclosure as applied above.

The recited Markush group renders the scope of claim 1 very broad.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Davis (US 6,137,173) is analogous art as per MPEP § 2141.01(a) since it is reasonably pertinent to the particular problem of etching the underside to provide contact to structures of the topside with which the inventor of the present invention is concerned. See especially Fig 15 to Fig 16 and col 4 ln 62-65. Davis also teaches thinning the substrate on the underside after coating the first substrate side. See especially Figs 8-9 and col 3 ln 45-54; and Figs 13-14 and col 4 ln 10-20.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew O. Arena whose telephone number is 571-272-5976. The examiner can normally be reached on M-F 8:30-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard T. Elms can be reached on 571- 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Sara Crane
Primary Examiner

Andrew O Arena
8 June 2007